

IDS Form PTO/SB/08: Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)				<b>Complete if Known</b> Application Number: 10/521,191 Filing Date: January 12, 2005 First Named Inventor: Takashi Yokokawa Art Unit: 2133 Examiner Name: RIZK, Samir Wadie Attorney Docket Number: 09812.0201-00000	
Sheet	1	of	1		

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No. <sup>1</sup>	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation
SR		Robert G. Gallager, <i>Low-Density Parity Check Codes</i> (M. I. T. Press 1963).	
SR		David J. C. MacKay, "Good Error-Correcting Codes Based on Very Sparse Matrices," <i>IEEE Transactions on Information Theory</i> , vol. 45, no. 2, pp. 399-431, March 1999.	
SR		Michael G. Luby, Michael Mitzenmacher, M. Amin Shokrollahi & Daniel A. Spielman, "Analysis of Low Density Codes and Improved Design Using Irregular Graphs," <i>Proceedings of ACM Symposium on Theory of Computing</i> , pp. 249-58 (1998).	
SR		C. Howland & A. Blanksby, "Parallel Decoding Architectures for Low Density Parity Check Codes," <i>Symposium on Circuits and Systems</i> , part IV, pp. 742-45 (2001).	
SR		Engling Yeo, Payam Pakzad, Borivoje Nikolic & Venkat Anantharam, "VLSI Architectures for Iterative Decoders in Magnetic Recording Channels," <i>IEEE Transactions on Magnetics</i> , vol. 37, no. 2, pp. 748-55, March 2001.	

Examiner Signature	/Samir Rizk/ (09/27/2006)	Date Considered	
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